09/353,938

L Number	Hits	Search Text	DB	Time stamp
1	534	pci same ((small adj form adj factor) or compact)	USPAT; US-PGPUB	2003/05/04 16:45
4	55	(remov$4 or detach$4) same (pci same ((small adj form adj factor) or compact))	USPAT; US-PGPUB	2003/05/04 16:45
7	46	(housing or card$1 or board$1) same ((remov$4 or detach$4) same (pci same ((small adj form adj factor) or compact)))	USPAT; US-PGPUB	2003/05/04 16:34
10	13	connector$1 same ((housing or card$1 or board$1) same ((remov$4 or detach$4) same (pci same ((small adj form adj factor) or compact))))	USPAT; US-PGPUB	2003/05/04 16:53
13	1		USPAT	2003/05/04 16:41
15	1		USPAT	2003/05/04 16:41
17	1		USPAT	2003/05/04 16:41
18	1		USPAT	2003/05/04 16:41
19	1		USPAT	2003/05/04 16:41
20	1		USPAT	2003/05/04 16:42
21	52	pci same ((small adj form adj factor) or compact)	EPO; JPO; DERWENT; IBM_TDB	2003/05/04 16:45
26	5	(remov$4 or detach$4) same (pci same ((small adj form adj factor) or compact))	EPO; JPO; DERWENT; IBM_TDB	2003/05/04 16:45
31	1	connector$1 same ((remov$4 or detach$4) same (pci same ((small adj form adj factor) or compact)))	EPO; JPO; DERWENT; IBM_TDB	2003/05/04 16:47
36	13	connector$1 same (pci same ((small adj form adj factor) or compact))	EPO; JPO; DERWENT; IBM_TDB	2003/05/04 16:48
41	71	connector$1 same (pci same ((small adj form adj factor) or compact))	USPAT; US-PGPUB	2003/05/04 16:54
44	9	41.ab,ti,clm.	USPAT; US-PGPUB	2003/05/04 16:57
47	0	pci same connector same modular same bay	USPAT; US-PGPUB	2003/05/04 16:58
50	111	connector$1 same modular same bay	USPAT; US-PGPUB	2003/05/04 16:58
53	1	pci same (connector$1 same modular same bay)	USPAT; US-PGPUB	2003/05/04 16:59
56	13	pci and (connector$1 same modular same bay)	USPAT; US-PGPUB	2003/05/04 17:13
59	2	((mini with pci) or (pci same ((small adj form adj factor) or compact))) and (connector$1 same modular same bay)	USPAT; US-PGPUB	2003/05/04 17:13

PGPUB-DOCUMENT-NUMBER: 20030033546

PGPUB-FILING-TYPE: new

DOCUMENT-IDENTIFIER: US 20030033546 A1

TITLE: System and method for graceful shutdown of host processor cards in a server system

PUBLICATION-DATE: February 13, 2003

INVENTOR-INFORMATION:

NAME	CITY	STATE	COUNTRY
RULE-47			
Bresniker, Kirk	Roseville	CA	US
Koch, James K.	Rocklin	CA	US

US-CL-CURRENT: 713/300

ABSTRACT:

A host processor card configured to be fitted into a server system includes a processor, and a memory coupled to the processor for storing an operating system. A power control line controls the power state of the host processor card. A graceful shutdown circuit is coupled to the processor and the power control line. The processor is configured to provide a graceful shutdown signal to the graceful shutdown circuit. The graceful shutdown circuit is configured to allow a graceful shutdown of the host processor card when the power control line indicates that the host processor card is to be powered down if the processor has provided the graceful shutdown signal.

---------- KWIC ---------

Summary of Invention Paragraph - BSTX (4):

[0002] **Compact** peripheral component interconnect (cPCI) is a standardized industrial form-factor implementation of the **PCI** Local bus I/O standard. As a physical standard, cPCI implements features that are designed to allow for the insertion and **removal** of I/O modules into a live chassis, for example blind mate **connectors** and staged length power and signal pins. In addition, as an electrical and protocol standard, there are features in cPCI that allow for inserted I/O modules to be recognized and configured, or **removed** modules to be de-configured by the host of the I/O bus and the software running on it. Pending **removal** of a peripheral I/O **card** is indicated by actuating an extractor handle, which has an integral switch to generate an electrical signal to the I/O bus host. **Cards** are energized after insertion or de-energized prior to **removal** by a hot swap controller, which is typically integrated into the host processor **card**.

PGPUB-DOCUMENT-NUMBER: 20030027434

PGPUB-FILING-TYPE: new

DOCUMENT-IDENTIFIER: US 20030027434 A1

TITLE: Low profile nic jumper solution using zif connector

PUBLICATION-DATE: February 6, 2003

INVENTOR-INFORMATION:

NAME	CITY	STATE	COUNTRY
RULE-47			
Homer, Steven S.	Tomball	TX	US
Atkinson, Lee	Houston	TX	US
Lakdawala, Rahul V.	Cypress	TX	US

US-CL-CURRENT: 439/61

ABSTRACT:

A connection technique for switchably and mutually exclusively coupling a plurality of device sets. The connection technique utilizes a low profile connector having multiple circuit sets, each of which is configured for mutually exclusive and removable insertion into a receptacle coupled to multiple devices. Each one of the multiple circuit sets, which is inserted into the receptacle, couples a desired set of the plurality of device sets.

---------- KWIC ---------

Detail Description Paragraph - DETX (13):

[0031] In the illustrated embodiment of FIG. 3, the computing component 162 is an integral component of the **compact** computing device 114. For example, the computing component may be an integral communication device or network **card**. In contrast, the computing component 160 is a **removable** computing component, such as a mini **PCI** network **card** or other PCMCIA **card**. Accordingly, the computing component 160 may be **removably** inserted into one of the slots 148 and 150 for utilization and interaction with the **compact** computing device 14 after performing the appropriate switch with the multi-directional **connector** 16 and the switchable multi-circuit **board** 18. It should also be noted that the electrical cables 154, 156, and 158 and the switchable multi-circuit **board** 18 may embody flexible printed circuits or other low profile circuitry to reduce space consumption in the **compact** computing device 14. As noted above, the multi-directional **connector** 16 may be a relatively low profile **connector,** such as a zero insertion force (ZIF) **connector,** adapted for the low profile or flexible circuitry of the switchable multi-circuit **board** 18 and the electrical cables 154-158 Accordingly, the present technique facilitates maximum flexibility and integration of the various computing components of the electrical connection system 10, the computing system 12, and the **compact** computing device 14 by using a low profile switchable connection system having multiple circuit sets.

US-PAT-NO: 6454585

DOCUMENT-IDENTIFIER: US 6454585 B1

TITLE: Low profile NIC jumper solution using ZIF connector

DATE-ISSUED: September 24, 2002

INVENTOR-INFORMATION:

NAME	CITY	STATE	ZIP CODE	COUNTRY
Homer; Steven S.	Tomball	TX	N/A	N/A
Atkinson; Lee	Houston	TX	N/A	N/A
Lakdawala; Rahul V.	Cypress	TX	N/A	N/A

US-CL-CURRENT: 439/218, 439/151 , 439/507

ABSTRACT:

A connection technique for switchably and mutually exclusively coupling a plurality of device sets. The connection technique utilizes a low profile connector having multiple circuit sets, each of which is configured for mutually exclusive and removable insertion into a receptacle coupled to multiple devices. Each one of the multiple circuit sets, which is inserted into the receptacle, couples a desired set of the plurality of device sets.

13 Claims, 5 Drawing figures

Exemplary Claim Number: 1

Number of Drawing Sheets: 3

---------- KWIC ---------

Detailed Description Text - DETX (13):

In the illustrated embodiment of FIG. 3, the computing component 162 is an integral component of the **compact** computing device 114. For example, the computing component may be an integral communication device or network **card**. In contrast, the computing component 160 is a **removable** computing component, such as a mini **PCI** network **card** or other PCMCIA **card**. Accordingly, the computing component 160 may be **removably** inserted into one of the slots 148 and 150 for utilization and interaction with the **compact** computing device 14 after performing the appropriate switch with the multi-directional **connector** 16 and the switchable multi-circuit **board** 18. It should also be noted that the electrical cables 154, 156, and 158 and the switchable multi-circuit **board** 18 may embody flexible printed circuits or other low profile circuitry to reduce space consumption in the **compact** computing device 14. As noted above, the multi-directional **connector** 16 may be a relatively low profile **connector,** such as a zero insertion force (ZIF) **connector,** adapted for the low profile or flexible circuitry of the switchable multi-circuit **board** 18 and the electrical cables 154-158. Accordingly, the present technique facilitates maximum flexibility and integration of the various computing components of the electrical connection system 10, the computing system 12, and the **compact** computing device 14 by using a low profile switchable connection system having multiple circuit sets.

US-PAT-NO: 6442034

DOCUMENT-IDENTIFIER: US 6442034 B1

TITLE: Front face of an electronics card and an electronics card

DATE-ISSUED: August 27, 2002

INVENTOR-INFORMATION:

NAME	CITY	STATE	ZIP CODE	COUNTRY
Ruque; Christian	Corbas	N/A	N/A	FR

US-CL-CURRENT: 361/754, 254/131 , 29/267 , 29/270 , 29/758 , 361/753 , 439/160 , 439/923

ABSTRACT:

In this front face of an electronics card designed to be inserted into a housing through an opening, at least one of the edges of which opening is provided with a notched bar, that portion of said front face which is to be disposed in the vicinity of said bar is provided with at least one abutment surface for abutting against a drive member engaged through the notch when inserting said card into the housing or when extracting it therefrom. The method consists in inserting a drive member through one of the notches in said bar, in causing said member to bear against an abutment surface, and in exerting a pivot force on said drive member to pivot it about the zone via which it bears against an edge of the notch, so that a force is transmitted to the front face, at the abutment surface, in a direction corresponding to inserting the card or to extracting the card.

11 Claims, 4 Drawing figures

Exemplary Claim Number: 11

Number of Drawing Sheets: 4

---------- KWIC ---------

Brief Summary Text - BSTX (4):

In view of recent developments in the connection techniques used to connect **cards,** such techniques including "**Compact PCI** bus" type devices or **connectors** designed to the IEC 1076-4-101 Standard, the forces required to put such **cards** in place in a corresponding **housing or to remove** them therefrom are large since such **cards** are difficult to move, in particular at the end of insertion or at the beginning of extraction.

US-PAT-NO: 6435897

DOCUMENT-IDENTIFIER: US 6435897 B1

TITLE: Compact PCI connector guide

DATE-ISSUED: August 20, 2002

INVENTOR-INFORMATION:

NAME	CITY	STATE	ZIP CODE	COUNTRY
Paul; Dieter	Anaheim	CA	N/A	N/A
Yuhan; James	Laguna Hills	CA	N/A	N/A

US-CL-CURRENT: 439/374, 439/567 , 439/701

ABSTRACT:

A **compact PCI connector** guide to be attached to a motherboard of a small computer system to surround a male **PCI connector** that is affixed to the motherboard. The **PCI connector** guide is adapted to accurately and automatically guide an incoming female **PCI connector** that is carried on a **detachable** peripheral printed circuit **board** into mating engagement with the male **PCI connector,** whereby the motherboard and the peripheral **board** are electrically interconnected with one another. The **PCI connector** guide has a body and flared lips projecting outwardly therefrom to automatically redirect the female **PCI connector** towards and into receipt by the male **PCI connector** without subjecting the contact pins of the male **PCI connector** to damage as a consequence of the male and female **PCI connectors** being misaligned with one another.

3 Claims, 9 Drawing figures

Exemplary Claim Number: 1

Number of Drawing Sheets: 3

---------- KWIC ---------

Abstract Text - ABTX (1):

A **compact PCI connector** guide to be attached to a motherboard of a small computer system to surround a male **PCI connector** that is affixed to the motherboard. The **PCI connector** guide is adapted to accurately and automatically guide an incoming female **PCI connector** that is carried on a **detachable** peripheral printed circuit **board** into mating engagement with the male **PCI connector,** whereby the motherboard and the peripheral **board** are electrically interconnected with one another. The **PCI connector** guide has a body and flared lips projecting outwardly therefrom to automatically redirect the female **PCI connector** towards and into receipt by the male **PCI connector** without subjecting the contact pins of the male **PCI connector** to damage as a consequence of the male and female **PCI connectors** being misaligned with one another.

Brief Summary Text - BSTX (3):

This invention relates to a **compact PCI** (peripheral component interconnect) **connector** guide that is attached to a motherboard of a small computer system to surround a male **PCI connector** in order to automatically and blindly direct an incoming female **PCI connector** that is carried on a **detachable** peripheral printed circuit **board** into a relatively quick and reliable mating engagement with the male **PCI connector,** whereby one or more electrical components on the peripheral **board** are interconnected with electrical components of the motherboard.

Brief Summary Text - BSTX (9):

In general terms, disclosed below is a **compact PCI connector** guide to be attached to the motherboard of a small computer system to surround a male **PCI connector** that is affixed to the motherboard in order to accurately and automatically direct an incoming female **PCI connector** that is carried on a **detachable** printed circuit **board** into a quick and reliable mating engagement with the male **PCI connector**. The **PCI connector** guide includes front, back and opposite side walls to define a hollow interior within which to receive the male **PCI connector when the connector** guide is attached to the motherboard. A flared lip projects outwardly from each of the front, back and side walls of the **connector** guide so as to extend above the male **PCI connector**.

Detailed Description Text - DETX (2):

The **compact PCI** (peripheral component interconnect) **connector** guide 2 which forms the present invention is now disclosed while referring to the drawings. As will be described in greater detail hereinafter, the **connector** guide 2 has a configuration which is particularly sized and adapted to permit the blind mating of a female **PCI connector** (designated 52 and best shown FIGS. 6-9) carried on a **detachable** peripheral printed circuit **board** 50 to a male **PCI connector** 62 that is electrically connected to a main motherboard 60 and surrounded by **connector** guide 2.

TDB-ACC-NO: NNRD429138

DISCLOSURE TITLE: Stand Alone Test Methodology for the Small Form Factor PCI Cards

PUBLICATION-DATA: IBM technical Disclosure Bulletin, January 2000, UK

ISSUE NUMBER: 429

PAGE NUMBER: 176

PUBLICATION-DATE: January 1, 2000 (20000101)

CROSS REFERENCE: 0374-4353-0-429-176

DISCLOSURE TEXT:

Disclosed is a device which allows the testing of small form factor **PCI** (Peripheral Component Interconnect) cards in a standard form factor **PCI** slot. In a standard **PCI** slot, the **small form factor PCI** card may be tested utilizing existing PC software, thus **removing** the need to create additional test software for in-situ testing.

There are a three **small form factor PCI** card industry standards; **Compact PCI,** Mini **PCI and PCI** Mezzanine Card (PMC). The device is a special **PCI** adapter which translates the **small form factor PCI** card **connector** into a standard **PCI** card **connector** so that the small card can be tested outside of the system for which it was designed. This special **PCI** adapter card is a passive device that will include **connectors** to accept the **small form factor** cards. It can have only one kind, or all three standards mating **connectors**.

A carefully designed card must be done to ensure compliance with the **PCI's** electrical specifications.

The advantages of this are twofold, first, the **small form factor** card is often a redesign of an existing **PCI** card and the test code written for that **PCI** card (DOS diagnostics for example) can be utilized without having to write special diagnostics to run in the **small form factor** platform. In many cases, the **small form factor** system will not be able to run a standard operating system for which the diagnostics already exist and additional development resource will be put into developing new software to test the card function.

The second advantage of this device is that it allows the developer to decouple the testing of the **small form factor** card from the testing of the system.

In many cases, this allows the parallel development of the system and adapter and can speed the development time for the adapter. Additionally, this allows the developer to isolate problems seen when coupling the **small form factor** card to the system by verifying the card in advance.

PAT-NO: JP411233199A

DOCUMENT-IDENTIFIER: JP 11233199 A

TITLE: BACK PLANE IN **COMPACT PCI** SYSTEM AND PLUG **CONNECTOR** FOR PLUG-IN CARD

PUBN-DATE: August 27, 1999

INVENTOR-INFORMATION:

NAME	COUNTRY
FRANZ, CHESHIKA	N/A

ASSIGNEE-INFORMATION:

NAME	COUNTRY
ERNI ELEKTROAPPAR GMBH	N/A

APPL-NO: JP10345811

APPL-DATE: December 4, 1998

INT-CL (IPC): H01R013/642, H01R023/02

ABSTRACT:

PROBLEM TO BE SOLVED: To simplify a plug connector working process and save assembly cost and storage cost.

SOLUTION: This connector consists of two modules M1, M2 arranged in a line at no intervals, and has a mechanical coding member CM, a plug piece M, and a socket piece to avoid the insertion error of one module. The modules M1, M2 positioned in a line on at least the edge surface side of the plug piece M and both modules of the socket piece are formed as a popular plastic molding product.

L Number	Hits	Search Text	DB	Time stamp
1	534	pci same ((small adj form adj factor) or compact)	USPAT; US-PGPUB	2003/05/04 16:45
4	55	(remov$4 or detach$4) same (pci same ((small adj form adj factor) or compact))	USPAT; US-PGPUB	2003/05/04 16:45
7	46	(housing or card$1 or board$1) same ((remov$4 or detach$4) same (pci same ((small adj form adj factor) or compact)))	USPAT; US-PGPUB	2003/05/04 16:34
10	13	connector$1 same ((housing or card$1 or board$1) same ((remov$4 or detach$4) same (pci same ((small adj form adj factor) or compact))))	USPAT; US-PGPUB	2003/05/04 16:45
13	1		USPAT	2003/05/04 16:41
15	1		USPAT	2003/05/04 16:41
17	1		USPAT	2003/05/04 16:41
18	1		USPAT	2003/05/04 16:41
19	1		USPAT	2003/05/04 16:41
20	1		USPAT	2003/05/04 16:42
21	52	pci same ((small adj form adj factor) or compact)	EPO; JPO; DERWENT; IBM_TDB	2003/05/04 16:45
26	5	(remov$4 or detach$4) same (pci same ((small adj form adj factor) or compact))	EPO; JPO; DERWENT; IBM_TDB	2003/05/04 16:45
31	1	connector$1 same ((remov$4 or detach$4) same (pci same ((small adj form adj factor) or compact)))	EPO; JPO; DERWENT; IBM_TDB	2003/05/04 16:47
36	13	connector$1 same (pci same ((small adj form adj factor) or compact))	EPO; JPO; DERWENT; IBM_TDB	2003/05/04 16:48

US-PAT-NO: 6190204

DOCUMENT-IDENTIFIER: US 6190204 B1

TITLE: Panel assembly for compact PCI system interface card

DATE-ISSUED: February 20, 2001

INVENTOR-INFORMATION:

NAME	CITY	STATE	ZIP CODE	COUNTRY
Huang; Tay-San	Taipei	N/A	N/A	TW

US-CL-CURRENT: 439/607, 439/359 , 439/573

ABSTRACT:

An improved structure of a interface card panel of a **compact PCI** system is disclosed. Wherein the panel of an interface card is assembled by welding an inner layered plate and an outer layered plate. The thickness of each layered plate is only half of the standard plate. The through holes of the inner layered plate have a radius only sufficient for receiving the screw rods of the fixing studs on the two ends of a D type **connector,** while the through holes for the outer layered plate have a radius sufficient for receiving the whole fixing studs, so that the fixing studs will completely pass through the outer layered plate, while the bodies thereof press the rim of the holes of the inner layered plate. Thus, other than the fixing points on the buckling bodies on the two ends thereof. By the fixing studs of the D type **connector,** a large fixing force is formed on the middle of the panel, and meanwhile, the strength of the panel is improved.

5 Claims, 5 Drawing figures

Exemplary Claim Number: 1

Number of Drawing Sheets: 5

---------- KWIC ---------

Abstract Text - ABTX (1):

An improved structure of a interface card panel of a **compact PCI** system is disclosed. Wherein the panel of an interface card is assembled by welding an inner layered plate and an outer layered plate. The thickness of each layered plate is only half of the standard plate. The through holes of the inner layered plate have a radius only sufficient for receiving the screw rods of the fixing studs on the two ends of a D type **connector,** while the through holes for the outer layered plate have a radius sufficient for receiving the whole fixing studs, so that the fixing studs will completely pass through the outer layered plate, while the bodies thereof press the rim of the holes of the inner layered plate. Thus, other than the fixing points on the buckling bodies on the two ends thereof. By the fixing studs of the D type **connector,** a large fixing force is formed on the middle of the panel, and meanwhile, the strength of the panel is improved.

Claims Text - CLTX (1):

1. A panel assembly for a **compact PCI** system interface card having at least one D-type **connector** comprising:

US-PAT-NO: 6129591

DOCUMENT-IDENTIFIER: US 6129591 A

TITLE: Multiway **connector** for backplanes and slide-in cards in **compact PCI** systems

DATE-ISSUED: October 10, 2000

INVENTOR-INFORMATION:

NAME	CITY	STATE	ZIP CODE	COUNTRY
Czeschka; Franz	Rechberghausen	N/A	N/A	DE

US-CL-CURRENT: 439/680, 439/491

ABSTRACT:

A multiway **connector** for backplanes and slide-in cards, for example, in so-called **compact PCI** systems, composed of two separate modules each arranged without spacing next to one another, wherein each of the modules has a mechanical coding piece for preventing incorrect insertions. At the two modules of the male multipoint **connector** resting against each other at end faces thereof as well as the modules of the female multipoint **connector** are constructed as a single-piece component of synthetic material.

5 Claims, 2 Drawing figures

Exemplary Claim Number: 1

Number of Drawing Sheets: 1

---------- KWIC ---------

Abstract Text - ABTX (1):

A multiway **connector** for backplanes and slide-in cards, for example, in so-called **compact PCI** systems, composed of two separate modules each arranged without spacing next to one another, wherein each of the modules has a mechanical coding piece for preventing incorrect insertions. At the two modules of the male multipoint **connector** resting against each other at end faces thereof as well as the modules of the female multipoint **connector** are constructed as a single-piece component of synthetic material.

TITLE - TI (1):

Multiway **connector** for backplanes and slide-in cards in **compact PCI** systems

Claims Text - CLTX (1):

1. A multiway **connector** for backplanes or slide-in cards for **compact PCI** systems, the **connector** comprising male and female multipoint **connectors,** each multipoint **connector** comprising at least two partial modules resting against each other at end faces thereof, wherein the partial modules of the male multipoint **connector** are comprised of a single-piece component of synthetic

material and the partial modules of the female multipoint **connector** are comprised of a single-piece synthetic material component, and wherein each **connector** comprises a mechanical coding piece for preventing incorrect insertions.

US-PAT-NO: 6552909

DOCUMENT-IDENTIFIER: US 6552909 B1

TITLE: Computer option bay having secondary access port with automatic sliding door mechanism

DATE-ISSUED: April 22, 2003

INVENTOR-INFORMATION:

NAME	CITY	STATE	ZIP CODE	COUNTRY
Liebenow; Frank	Dakota Dunes	SD	N/A	N/A

US-CL-CURRENT: 361/725, 361/683 , 361/686 , 361/724

ABSTRACT:

A computer system having a housing including an option bay into which a modular option device may be removably inserted is disclosed. The option bay includes a secondary access port providing access to the modular option device for uncluttered connection of lines and easy access to control functions. The secondary access port may be covered by a sliding door that opens automatically upon insertion of selected modular option devices into the option bay.

27 Claims, 7 Drawing figures

Exemplary Claim Number: 1

Number of Drawing Sheets: 4

---------- KWIC ---------

Detailed Description Text - DETX (6):

A secondary access port door 114 may cover the secondary access port 110. Preferably, the secondary access port door 114 prevents exposure of the option **bay** 108 to environmental contaminants via the secondary access port 110 when no **modular** option device 118 & 122 is inserted therein. The secondary access port door 114 may include a catch 116 keyed to slide within a channel 120, or, alternatively, engage a notch 126 in a **modular** option device 118 & 122. When a properly keyed **modular** option device (e.g., **modular** option device 122) is inserted into the option **bay** 108, the catch 116 engages the notch 126 and is forced inwardly (e.g., into the option **bay** 108) causing the secondary access port door 114 to be at least partially opened. This allows access by the user, via the secondary access port 110, to features 124 such as **connectors,** jacks, controls, indicators, or the like mounted to the side of the **modular** option device 122.

Detailed Description Text - DETX (7):

For example, as shown in FIG. 1, a first **modular** option device 122 may be removably inserted into the option **bay** 108. This **modular** option device 122 may be, for example, a modem, ac power supply, etc., having a feature 124 such as a **connector,** port, or the like which requires connection of a line or cable via the secondary access port 110. Thus, the first **modular** option device 122 may

include a notch 126 formed in its housing 162. When the first **modular** option device 122 is inserted into the option **bay** 108, this notch 126 may be engaged by the catch 116 extending from the secondary access port door 114 causing the door 114 to be urged from a fully closed position to a fully opened position via the tab/notch contact.

Detailed Description Text - DETX (11):

As shown in FIG. 3, one or more or guides 136 may guide a selected **modular** option device 118, 122, or 130 (FIGS. 1 and 2) as it is inserted within the option **bay** 108 so that the device is properly positioned therein when fully inserted. The option **bay** 108 may include apparatus (not shown) for interconnecting the **modular** option device 118, 122 & 130 (FIGS. 1 and 2) with the computer system 100. This apparatus may comprise a conventional **connector** (e.g., a multiple pin **connector,** spring contact type **connector,** banana plug type **connector,** etc.) mounted to the **modular** option device 118, 122, & 130 (FIGS. 1 and 2) for mating with a corresponding **connector** mounted within the option **bay** 108. The computer system 100 may further comprise conventional apparatus (not shown) for removing or ejecting the **modular** option device 118, 122, & 130 (FIGS. 1 and 2) from the option **bay** 108.

Detailed Description Text - DETX (15):

Referring now to FIGS. 4A through 4C, the secondary access port and secondary access port door are shown. The secondary access port door 114 may slide between a fully closed position, shown in FIG. 4A, and a fully opened position, shown in FIG. 4B, to allow access by the user to one or more coupling devices 132, ports 146, or ac power **connectors** 150 via the secondary access port 110. As shown in FIG. 4A, the secondary access port door 114 may be held in a fully closed position when the option **bay** is empty or when a **modular** option device having no external coupling devices is inserted therein. When a **modular** option device (such as fourth **modular** option device 144) is inserted in the option **bay,** as shown in FIG. 4B, the secondary access port door 114 may be moved to the fully opened position allowing access to a port 146 such as a multiple pin **connector** or the like. Alternatively, a fifth **modular** option device 148 may cause the secondary access port door 114 to be only partially opened as shown in FIG. 4C.

Detailed Description Text - DETX (16):

Referring now to FIG. 5, a block diagram of a typical computer system which may employ the present invention is illustrated. The computer system 200 is controlled by a central processing system 202. The central processing system 202 includes a central processing unit such as a microprocessor or microcontroller for executing programs, performing data manipulations and controlling the tasks of the computer system 200. Communication with the central processing system 202 is implemented through a system bus 210 for transferring information among the components of the computer system 200. The bus 210 may include a data channel for facilitating information transfer between storage and other peripheral components of the hardware system. The bus 210 further provides the set of signals required for communication with the central processing system 202 including a data bus, address bus, and control bus. The bus 210 may comprise any state of the art bus architecture according to promulgated standards, for example industry standard architecture (ISA), extended industry standard architecture (EISA), Micro Channel Architecture (MCA), peripheral component interconnect (**PCI**) local bus, standards promulgated by the Institute of Electrical and Electronics Engineers (IEEE) including IEEE 488 general-purpose interface bus (GPIB), IEEE 696/S-100, and so on. Other components of the computer system 200 include main memory 204, auxiliary memory 206, and an auxiliary processing system 208 as required. The main memory 204

provides storage of instructions and data for programs executing on the central processing system 202. The main memory 204 is typically semiconductor based memory such as dynamic random access memory (DRAM) and or static random access memory (SRAM). The auxiliary memory 206 provides storage of instructions and data that are loaded into the main memory 204 before execution. The auxiliary memory 206 may include semiconductor based memory such as read-only memory (ROM), programmable read-only memory (PROM) erasable programmable read-only memory (EPROM), electrically erasable read-only memory (EEPPOM), or flash memory (block oriented memory similar to EEPROM). The auxiliary memory 206 may also include a variety of non-semiconductor based memories, including but not limited to magnetic tape, drum, floppy disk, hard disk, optical, laser disk, compact disc read-only memory (CD-ROM), digital versatile disk read-only memory (DVD-ROM), digital versatile disk random-access memory (DVD-RAM), etc. Other varieties of memory devices are contemplated as well. The computer system 200 may optionally include an auxiliary processing system 208 which may be a digital signal processor (a special-purpose microprocessor having an architecture suitable for fast execution of signal processing algorithms), a back-end processor (a slave processor subordinate to the main processing system), an additional microprocessor or controller for dual or multiple processor systems, or a coprocessor.

US-PAT-NO: 6307745

DOCUMENT-IDENTIFIER: US 6307745 B1

TITLE: Computer option bay having secondary access port with automatic sliding door mechanism

DATE-ISSUED: October 23, 2001

INVENTOR-INFORMATION:

NAME	CITY	STATE	ZIP CODE	COUNTRY
Liebenow; Frank	Dakota Dunes	SD	N/A	N/A

US-CL-CURRENT: 361/686, 361/680 , 361/681 , 361/682 , 361/724 , 361/725 , 361/726 , 361/727

ABSTRACT:

A computer system having a housing including an option bay into which a modular option device may be removably inserted is disclosed. The option bay includes a secondary access port providing access to the modular option device for uncluttered connection of lines and easy access to control functions. The secondary access port may be covered by a sliding door which opens automatically upon insertion of selected modular option devices into the option bay.

27 Claims, 7 Drawing figures

Exemplary Claim Number: 1

Number of Drawing Sheets: 4

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Detailed Description Text - DETX (6):

A secondary access port door 114 may cover the secondary access port 110. Preferably, the secondary access port door 114 prevents exposure of the option **bay** 108 to environmental contaminants via the secondary access port 110 when no **modular** option device 118 & 122 is inserted therein. The secondary access port door 114 may include a catch 116 keyed to slide within a channel 120, or, alternatively, engage a notch 126 in a **modular** option device 118 & 122. When a properly keyed **modular** option device (e.g., **modular** option device 122) is inserted into the option **bay** 108, the catch 116 engages the notch 126 and is forced inwardly (e.g., into the option **bay** 108) causing the secondary access port door 114 to be at least partially opened. This allows access by the user, via the secondary access port 110, to features 124 such as **connectors,** jacks, controls, indicators, or the like mounted to the side of the **modular** option device 122.

Detailed Description Text - DETX (7):

For example, as shown in FIG. 1, a first **modular** option device 122 may be removably inserted into the option **bay** 108. This **modular** option device 122 may be, for example, a modem, ac power supply, etc., having a feature 124 such as a **connector,** port, or the like which requires connection of a line or cable via

the secondary access port 110. Thus, the first **modular** option device 122 may include a notch 126 formed in its housing 162. When the first **modular** option device 122 is inserted into the option **bay** 108, this notch 126 may be engaged by the catch 116 extending from the secondary access port door 114 causing the door 114 to be urged from a fully closed position to a fully opened position via the tab/notch contact.

Detailed Description Text - DETX (11):

As shown in FIG. 3, one or more or guides 136 may guide a selected **modular** option device 118, 122, or 130 (FIGS. 1 and 2) as it is inserted within the option **bay** 108 so that the device is properly positioned therein when fully inserted. The option **bay** 108 may include apparatus (not shown) for interconnecting the **modular** option device 118, 122, & 130 (FIGS. 1 and 2) with the computer system 100. This apparatus may comprise a conventional **connector** (e.g., a multiple pin **connector,** spring contact type **connector,** banana plug type **connector,** etc) mounted to the **modular** option device 118, 122, & 130 (FIGS. 1 and 2) for mating with a corresponding **connector** mounted within the option **bay** 108. The computer system 100 may further comprise conventional apparatus (not shown) for removing or ejecting the **modular** option device 118, 122, & 130 (FIGS. 1 and 2) from the option **bay** 108.

Detailed Description Text - DETX (15):

Referring now to FIGS. 4A through 4C, the secondary access port and secondary access port door are shown. The secondary access port door 114 may slide between a fully closed position, shown in FIG. 4A, and a fully opened position, shown in FIG. 4B, to allow access by the user to one or more coupling devices 132, ports 146, or ac power **connectors** 150 via the secondary access port 110. As shown in FIG. 4A, the secondary access port door 114 may be held in a fully closed position when the option **bay** is empty or when a **modular** option device having no external coupling devices is inserted therein. When a **modular** option device (such as fourth **modular** option device 144) is inserted in the option **bay,** as shown in FIG. 4B, the secondary access port door 114 may be moved to the fully opened position allowing access to a port 146 such as a multiple pin **connector** or the like. Alternatively, a fifth **modular** option device 148 may cause the secondary access port door 114 to be only partially opened as shown in FIG. 4C.

Detailed Description Text - DETX (16):

Referring now to FIG. 5, a block diagram of a typical computer system which may employ the present invention is illustrated. The computer system 200 is controlled by a central processing system 202. The central processing system 202 includes a central processing unit such as a microprocessor or microcontroller for executing programs, performing data manipulations and controlling the tasks of the computer system 200. Communication with the central processing system 202 is implemented through a system bus 210 for transferring information among the components of the computer system 200. The bus 210 may include a data channel for facilitating information transfer between storage and other peripheral components of the hardware system. The bus 210 further provides the set of signals required for communication with the central processing system 202 including a data bus, address bus, and control bus. The bus 210 may comprise any state of the art bus architecture according to promulgated standards, for example industry standard architecture (ISA), extended industry standard architecture (EISA), Micro Channel Architecture (MCA), peripheral component interconnect (**PCI**) local bus, standards promulgated by the Institute of Electrical and Electronics Engineers (IEEE) including IEEE 488 general-purpose interface bus (GPIB), IEEE 696/S-100, and so on. Other components of the computer system 200 include main memory 204, auxiliary memory

206, and an auxiliary processing system 208 as required. The main memory 204 provides storage of instructions and data for programs executing on the central processing system 202. The main memory 204 is typically semiconductor based memory such as dynamic random access memory (DRAM) and or static random access memory (SRAM). The auxiliary memory 206 provides storage of instructions and data that are loaded into the main memory 204 before execution. The auxiliary memory 206 may include semiconductor based memory such as read-only memory (ROM), programmable read-only memory (PROM) erasable programmable read-only memory (EPROM), electrically erasable read-only memory (EEPROM), or flash memory (block oriented memory similar to EEPROM). The auxiliary memory 206 may also include a variety of non-semiconductor based memories, including but not limited to magnetic tape, drum, floppy disk, hard disk, optical, laser disk, compact disc read-only memory (CD-ROM), digital versatile disk read-only memory (DVD-ROM), digital versatile disk random-access memory (DVD-RAM), etc. Other varieties of memory devices are contemplated as well. The computer system 200 may optionally include an auxiliary processing system 208 which may be a digital signal processor (a special-purpose microprocessor having an architecture suitable for fast execution of signal processing algorithms), a back-end processor (a slave processor subordinate to the main processing system), an additional microprocessor or controller for dual or multiple processor systems, or a coprocessor.

US-PAT-NO: 5963431

DOCUMENT-IDENTIFIER: US 5963431 A

TITLE: Desktop computer having enhanced motherboard/riser card assembly configuration

DATE-ISSUED: October 5, 1999

INVENTOR-INFORMATION:

NAME	CITY	STATE	ZIP CODE	COUNTRY
Stancil; Charles J.	Tomball	TX	N/A	N/A

US-CL-CURRENT: 361/803, 361/785 , 361/788 , 361/796 , 439/61

ABSTRACT:

A desktop computer system is provided in which a motherboard is mounted within a computer chassis atop a tray which is rearwardly slidable out of a rear wall opening in the chassis to provide access to the motherboard. I/O cables are coupled to I/O connectors mounted on a rear end edge of the motherboard, and a connector socket extending along a side edge portion of the motherboard removably receives a bottom side edge connector portion of a riser card which transversely projects upwardly from the motherboard. All cable connections from internal computer devices are made directly to the riser card instead of to the motherboard. Accordingly, all that is necessary to provide access to the motherboard is to upwardly unseat the riser card from the motherboard and then slide the motherboard, with the I/O cables still connected thereto, rearwardly out of the chassis on the tray. Using a single PHY host controller bus driver disposed on the riser card, the motherboard/riser card assembly economically provides support for multiple device bays within the computer.

32 Claims, 5 Drawing figures

Exemplary Claim Number: 1

Number of Drawing Sheets: 3

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Brief Summary Text - BSTX (7):

When the LPX motherboard/riser card form factor is utilized, the riser board contains the **PCI** and ISA expansion slots, and a bottom connection edge portion of the riser card removably plugs into an elongated connector socket generally centrally disposed on the top side of the motherboard. The motherboard is disposed within the computer housing chassis and removably screwed to the bottom wall of the chassis. The necessary I/O cables (for the serial port, parallel port, keyboard, mouse, etc.) extend inwardly through the back side of the computer housing and are removably plugged into suitable connectors mounted on a rear edge portion of the motherboard. Cables from various internal components of the computer (for example, the power supply unit, IDE, floppy drive, speaker, etc.) are removably secured to suitable connectors on the top side of the motherboard.

Brief Summary Text - BSTX (12):

Furthermore, neither the LPX form factor (either in its standard configuration or its modified configuration discussed above) nor the NLX motherboard/riser card form factor is particularly well suited for use in a computer which incorporates more than one "device **bay**" therein. A device **bay** is basically an internal **bay** area within the computer chassis into which a **modular** computer device (such as a CD ROM drive, a hard drive or a floppy drive) may be operatively and removably inserted from the exterior of the computer. The insertable **modular** device typically has a **connector** on its back end which mates with a corresponding **bay connector** structure in response to insertion of the device into the **bay, the bay** structure **connector** structure, in turn, being cabled to the motherboard or the riser card depending upon which motherboard/riser card form factor is being utilized.

Detailed Description Text - DETX (9):

Such internal components include three vertically stacked device bays 88,90 and 92, the upper two of which are connected to the riser card 46 respectively by the internal component cables 84 and 86 that are secured to **connectors** (such as the illustrated **connector** 94) positioned on the rear or inner vertical walls of the device bays. The preferred placement of the motherboard **connector** socket 66 closely adjacent the motherboard side edge 58 advantageously reduces the necessary lengths of the **connector** cables 78-86. Each device **bay** has an open front end through which a **modular** device (such as a CD ROM drive, a floppy drive, a hard drive or the like) may be rearwardly inserted into the **bay, the modular** device (not shown) having on its rear side a **connector** which mates with the device **bay** rear wall **connector** to link the inserted **modular** device to the riser card 46 (and thus the motherboard 44) via the corresponding device **bay** cable plugged into the riser card 46.

US-PAT-NO: 5822547

DOCUMENT-IDENTIFIER: US 5822547 A

TITLE: Method and apparatus for providing a portable computer with hot pluggable modular bays

DATE-ISSUED: October 13, 1998

INVENTOR-INFORMATION:

NAME	CITY	STATE	ZIP CODE	COUNTRY
Boesch; Shannon C.	Georgetown	TX	N/A	N/A
Haley; Charles L.	Temple	TX	N/A	N/A

US-CL-CURRENT: 710/302, 710/107 , 710/48

ABSTRACT:

A computer system 10, such as a notebook computer, uses a modular bay 12 to receive optional devices 14. Buffer circuits 36 selectively isolate the device 14 in the modular bay from respective buses 34. An SMI handler, or similar executable routine, recognizes events which affect the modular bay 12 (such as insertion or removal of a device 14 from the modular bay 12), and performs the necessary routines to re-enumerate the system so that the device 14 is properly connected to its bus 34 and that the system software is aware of the hardware connected to computer 10.

9 Claims, 5 Drawing figures

Exemplary Claim Number: 1

Number of Drawing Sheets: 3

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Detailed Description Text - DETX (5):

In operation, the **modular** devices 14 each include a **connector** which connects to a corresponding **connector** disposed in the back of the **modular bay** 12 (see FIG. 2). For example, a standard 80-pin **connector** can be used to electrically couple the **modular** device 14 with the system electronics of the computer. To ensure a reliable connection, a mechanical latch (not shown) holds the **modular** device 14 in the **modular bay** 12 once the **modular** device 14 is fully seated in the **bay**.

Detailed Description Text - DETX (8):

FIG. 2 illustrates a block diagram of the computer system 10. The system processing circuitry 22 includes, in part, a central processing unit (CPU) 24, a system BIOS 26, main memory 28, floppy controller 29, video/graphics controller 30, frame buffer 32 and modem 33 (including asynchronous I/O circuitry). The system processing circuitry 22 communicates with the keyboard 18 and the display 20. In connection with the **modular bay** 12, there are three buses 34 coupled between the system processing circuitry 22 and the **modular bay** 12, referenced individually as the IDE bus 34a, the floppy bus 34b and the telephony bus 34c. Each of the buses 34 is coupled to a respective buffer 36,

referenced individually as buffers 36a-c. The buffers 36 couple the buses 34 to shared bus 37. Shared bus 37 is connected to **connector** 38, which is disposed in the **modular bay** 12.

Detailed Description Text - DETX (14):

Power is supplied to the device 14 in the **modular bay** 12 through a transistor 54 having a control node coupled to MBPower pin of the bus control logic 40. When MBPower is at a high logic level, power flows from V.sub.cc to the device 14 in the **modular bay** 12. If the device 14 is a battery, it will couple to a separate **connector** (not shown) which works in conjunction with the primary battery.

Detailed Description Text - DETX (17):

For purposes of illustration, it is presumed that all four bit lines of the ID signal are connected to V.sub.cc via pull up resistors (not shown). Accordingly, when no device 14 is mounted in the **modular bay** 12, ID is set to a logical "1111". All devices 14, therefore, would have an ID in which at least one bit was a logical "0", which can be implemented by grounding one or more of the lines of cable 44 which make up the ID signal. When an initial connection is made between device 14 and the computer-side **connector** 38 (even before the device 14 is fully latched into the **modular bay** 12), the bus control logic 40 can identify the mounting of the device responsive to any one of the ID pins undergoing a transition from a logical "1" to a logical "0". Similarly, the bus control logic 40 can identify the complete removal of a device 14 from the **modular bay** 12 when all four ID bits are set to a logical "1".

Detailed Description Text - DETX (29):

Many notebook systems provide for a docking station. A docking station allows connection of the computer 10 to devices which may not be suitable for portable use. For example, the docking station may provide an interface and a physical connection to a local area network. It may also provide standard bus slots (such as Industry Standard Architecture (ISA) or Peripheral Connect Interface (**PCI**) slots) for the user to add peripheral cards, such as advanced video cards or sound cards. The system designer may chose to disable the modular bay (by disabling all buffers 36 and re-enumerating the system) while the computer 10 is connected to a docking station.

Detailed Description Text - DETX (31):

The structure for the **modular** device 14, described above, allows a single **connector** type to be used with a plurality of component types, so that off-the-shelf components can be used in the housing 45 to provide many different functions for the **modular bay** 12. The **connector** 42 has a number of pins which is equal to or in excess of the number of bits in the largest bus 34 plus the number control signal bits for ID plus bits reserved for future expansion. The cable 44 provides the mechanism for mapping various **connector** types associated with the different components which may be used (for example, floppy drives and hard disks use different **connector** types) to the **connector** 42. Similarly, shared bus 37 will be connected to only one of the buses 36 at a time; therefore, shared bus 37 need only be as wide as the widest bus 36.

Detailed Description Text - DETX (32):

The computer system 10 provides significant advantages over the prior art. The shared bus structure shown FIG. 2 provides a great cost and space savings,

since it greatly reduces the number of pins which would otherwise be necessary to accommodate various components, such as those discussed above. The reduction of the **connector** pin count (relative to individual **connectors** for each type of device supported by the **modular bay**) also provides an important mechanical benefit since the lower pin count reduces the total insertion and removal force needed to mate and separate the **connectors** 38 and 42.

US-PAT-NO: 5799068

DOCUMENT-IDENTIFIER: US 5799068 A

TITLE: Smart phone integration with computer systems

DATE-ISSUED: August 25, 1998

INVENTOR-INFORMATION:

NAME	CITY	STATE	ZIP CODE	COUNTRY
Kikinis; Dan	Saratoga	CA	N/A	N/A
Dornier; Pascal	Sunnyvale	CA	N/A	N/A
Seiler; William J.	Scotts Valley	CA	N/A	N/A

US-CL-CURRENT: 379/93.06, 379/357.01 , 710/13 , 710/301

ABSTRACT:

A business telephone system employs digital signal processing in a digital telephone having a serial link for connection to a general-purpose computer. The Smart Phone is the central intelligence for the system, which may utilize a PBX connected in a LAN network to multiple computers, including file servers, and each computer may have one or more Smart Phones connected. In one embodiment, docking bays in the phone provide an ability to interchange finctional modules, including DSP modules. The docking bays and functional modules may be configured to PCMCIA standards. In another embodiment, a docking bay, which may also be PCMCIA, has a physical window allowing access to an input area on a docked module, wherein the docked module is an intelligent module with a CPU, a memory, and a bus structure, affording control of the smart phone and the entire system through the input interface of the docked module. In various embodiments the external form of the system may vary, and in one embodiment, the smart phone elements are integrated with a desktop or a portable computer having docking bays to receive and connect functional modules, such a DSP modules and/or an intelligent module.

7 Claims, 54 Drawing figures

Exemplary Claim Number: 6

Number of Drawing Sheets: 46

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Detailed Description Text - DETX (64):

Host bus connector 1014 is a part of a host interface which comprises a bus structure 1026 for providing connection to the host in docked mode, as described above. In a preferred embodiment, the host interface is according to PCMCIA Type II, Rev. 3 standard, which is capable of communication either in PCMCIA mode or in a mode similar to **PCI** mode. **PCI** mode refers to a high-speed intermediate bus protocol being developed by Intel corporation, expected to become a standard bus architecture and protocol in the industry. The physical interface at the host in this embodiment is a slot-like docking bay, as is typical of know docking bays for PCMCIA devices. This docking bay may be implemented as a docking box, a built-in unit like a floppy-drive unit, or it may take some other form.

Detailed Description Text - DETX (209):

Power modules such as module 2111 may be plugged into a **connector** on a charging module separate from the notebook computer, using the same **connector** used for plugging into the Notebus via a module **bay** of framework 2011, and recharged for later use with a **modular** notebook computer according to the invention. This allows a user to keep spare power modules ready for use, and to recharge modules without connecting the computer itself to a charging unit. Moreover, the provision of power modules allows a user to provide more or less portable time to the notebook computer by using one or more than one power module.

US-PAT-NO: 5708840

DOCUMENT-IDENTIFIER: US 5708840 A

TITLE: Micro personal digital assistant

DATE-ISSUED: January 13, 1998

INVENTOR-INFORMATION:

NAME	CITY	STATE	ZIP CODE	COUNTRY
Kikinis; Dan	Saratoga	CA	N/A	N/A
Dornier; Pascal	Sunnyvale	CA	N/A	N/A
Seiler; William J.	Scotts Valley	CA	N/A	N/A

US-CL-CURRENT: 708/105, 341/137 , 345/169

ABSTRACT:

A personal digital assistant module with a local CPU, memory, and I/O interface has a host interface comprising a bus connected to the local CPU and a connector at a surface of the personal digital assistant for interfacing to a bus connector of a host general-purpose computer, providing direct bus communication between the personal digital assistant and the host general-purpose computer. In an embodiment, the personal digital assistant also has a means for storing a security code. The personal digital assistant according to the invention forms a host/satellite combination with a host computer having a docking bay, wherein upon docking a docking protocol controls access by the host to memory of the personal digital assistant based on one or more passwords provided by a user to the host. In another embodiment the personal digital assistant also has an expansion port connected to the local CPU, and expansion peripheral devices may be connected and operated through the expansion port. Also disclosed are various embodiments for host systems compatible with personal digital assistants according to the invention, and a scanner system useful with displays of both personal digital assistants and hosts.

14 Claims, 50 Drawing figures

Exemplary Claim Number: 1

Number of Drawing Sheets: 43

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Detailed Description Text - DETX (13):

Host bus connector 14 is a part of a host interface which comprises a bus structure 26 for providing connection to the host in docked mode, as described above. In a preferred embodiment, the host interface is according to PCMCIA Type II, Rev. 3 standard, which is capable of communication either in PCMCIA mode or in a mode similar to **PCI** mode. **PCI** mode refers to a high-speed intermediate bus protocol being developed by Intel corporation, expected to become a standard bus architecture and protocol in the industry. The physical interface at the host in this embodiment is a slot-like docking bay, as is typical of know docking bays for PCMCIA devices. This docking bay may be implemented as a docking box, a built-in unit like a floppy-drive unit, or it may take some other form.

Detailed Description Text - DETX (159):

Power modules such as module 1111 may be plugged into a **connector** on a charging module separate from the notebook computer, using the same **connector** used for plugging into the Notebus via a module **bay** of framework 1011, and recharged for later use with a **modular** notebook computer according to the invention. This allows a user to keep spare power modules ready for use, and to recharge modules without connecting the computer itself to a charging unit. Moreover, the provision of power modules allows a user to provide more or less portable time to the notebook computer by using one or more than one power module.

US-PAT-NO: 5634080

DOCUMENT-IDENTIFIER: US 5634080 A

TITLE: Hand-held portable computer having an electroluminescent flat-panel display with pixel elements at right angles to the plane of the display and an excitation direction parallel to the plane of the display

DATE-ISSUED: May 27, 1997

INVENTOR-INFORMATION:

NAME	CITY	STATE	ZIP CODE	COUNTRY
Kikinis; Dan	Sratoga	CA	N/A	N/A
Dornier; Pascal	Sunnyvale	CA	N/A	N/A
Seiler; William J.	Scotts Valley	CA	N/A	N/A

US-CL-CURRENT: 710/73, 345/156 , 345/45 , 361/686 , 455/575 , 709/253 , 710/303

ABSTRACT:

A personal digital assistant module with a local CPU, memory, and I/O interface has a host interface comprising a bus connected to the local CPU and a connector at a surface of the personal digital assistant for interfacing to a bus connector of a host general-purpose computer, providing direct bus communication between the personal digital assistant and the host general-purpose computer. In an embodiment, the personal digital assistant also stores a security code. The personal digital assistant according to the invention forms a host/satellite combination with a host computer having a docking bay, wherein upon docking a docking protocol controls access by the host to memory of the personal digital assistant based on one or more passwords provided by a user to the host. In another embodiment the personal digital assistant also has an expansion port connected to the local CPU, and expansion peripheral devices may be connected and operated through the expansion port.

13 Claims, 74 Drawing figures

Exemplary Claim Number: 1

Number of Drawing Sheets: 53

---------- KWIC ---------

Detailed Description Text - DETX (13):

Host bus connector 14 is a part of a host interface which comprises a bus structure 26 for providing connection to the host in docked mode, as described above. In a preferred embodiment, the host interface is according to PCMCIA Type II, Rev. 3 standard, which is capable of communication either in PCMCIA mode or in a mode similar to **PCI** mode. **PCI** mode refers to a high-speed intermediate bus protocol being developed by Intel corporation, expected to become a standard bus architecture and protocol in the industry. The physical interface at the host in this embodiment is a slot-like docking bay, as is typical of know docking bays for PCMCIA devices. This docking bay may be implemented as a docking box, a built-in unit like a floppy-drive unit, or it may take some other form.

Detailed Description Text - DETX (252):

Power modules such as module 2111 may be plugged into a **connector** on a charging module separate from the notebook computer, using the same **connector** used for plugging into the Notebus via a module **bay** of framework 2011, and recharged for later use with a **modular** notebook computer according to the invention. This allows a user to keep spare power modules ready for use, and to recharge modules without connecting the computer itself to a charging unit. Moreover, the provision of power modules allows a user to provide more or less portable time to the notebook computer by using one or more than one power module.

US-PAT-NO: 6307745

DOCUMENT-IDENTIFIER: US 6307745 B1

TITLE: Computer option bay having secondary access port with automatic sliding door mechanism

DATE-ISSUED: October 23, 2001

INVENTOR-INFORMATION:

NAME	CITY	STATE	ZIP CODE	COUNTRY
Liebenow; Frank	Dakota Dunes	SD	N/A	N/A

US-CL-CURRENT: 361/686, 361/680 , 361/681 , 361/682 , 361/724 , 361/725 , 361/726 , 361/727

ABSTRACT:

A computer system having a housing including an option bay into which a modular option device may be removably inserted is disclosed. The option bay includes a secondary access port providing access to the modular option device for uncluttered connection of lines and easy access to control functions. The secondary access port may be covered by a sliding door which opens automatically upon insertion of selected modular option devices into the option bay.

27 Claims, 7 Drawing figures

Exemplary Claim Number: 1

Number of Drawing Sheets: 4

---------- KWIC ---------

Detailed Description Text - DETX (6):

A secondary access port door 114 may cover the secondary access port 110. Preferably, the secondary access port door 114 prevents exposure of the option **bay** 108 to environmental contaminants via the secondary access port 110 when no **modular** option device 118 & 122 is inserted therein. The secondary access port door 114 may include a catch 116 keyed to slide within a channel 120, or, alternatively, engage a notch 126 in a **modular** option device 118 & 122. When a properly keyed **modular** option device (e.g., **modular** option device 122) is inserted into the option **bay** 108, the catch 116 engages the notch 126 and is forced inwardly (e.g., into the option **bay** 108) causing the secondary access port door 114 to be at least partially opened. This allows access by the user, via the secondary access port 110, to features 124 such as **connectors,** jacks, controls, indicators, or the like mounted to the side of the **modular** option device 122.

Detailed Description Text - DETX (7):

For example, as shown in FIG. 1, a first **modular** option device 122 may be removably inserted into the option **bay** 108. This **modular** option device 122 may be, for example, a modem, ac power supply, etc., having a feature 124 such as a **connector,** port, or the like which requires connection of a line or cable via

the secondary access port 110. Thus, the first **modular** option device 122 may include a notch 126 formed in its housing 162. When the first **modular** option device 122 is inserted into the option **bay** 108, this notch 126 may be engaged by the catch 116 extending from the secondary access port door 114 causing the door 114 to be urged from a fully closed position to a fully opened position via the tab/notch contact.

Detailed Description Text - DETX (11):

As shown in FIG. 3, one or more or guides 136 may guide a selected **modular** option device 118, 122, or 130 (FIGS. 1 and 2) as it is inserted within the option **bay** 108 so that the device is properly positioned therein when fully inserted. The option **bay** 108 may include apparatus (not shown) for interconnecting the **modular** option device 118, 122, & 130 (FIGS. 1 and 2) with the computer system 100. This apparatus may comprise a conventional **connector** (e.g., a multiple pin **connector,** spring contact type **connector,** banana plug type **connector,** etc) mounted to the **modular** option device 118, 122, & 130 (FIGS. 1 and 2) for mating with a corresponding **connector** mounted within the option **bay** 108. The computer system 100 may further comprise conventional apparatus (not shown) for removing or ejecting the **modular** option device 118, 122, & 130 (FIGS. 1 and 2) from the option **bay** 108.

Detailed Description Text - DETX (15):

Referring now to FIGS. 4A through 4C, the secondary access port and secondary access port door are shown. The secondary access port door 114 may slide between a fully closed position, shown in FIG. 4A, and a fully opened position, shown in FIG. 4B, to allow access by the user to one or more coupling devices 132, ports 146, or ac power **connectors** 150 via the secondary access port 110. As shown in FIG. 4A, the secondary access port door 114 may be held in a fully closed position when the option **bay** is empty or when a **modular** option device having no external coupling devices is inserted therein. When a **modular** option device (such as fourth **modular** option device 144) is inserted in the option **bay,** as shown in FIG. 4B, the secondary access port door 114 may be moved to the fully opened position allowing access to a port 146 such as a multiple pin **connector** or the like. Alternatively, a fifth **modular** option device 148 may cause the secondary access port door 114 to be only partially opened as shown in FIG. 4C.

Detailed Description Text - DETX (16):

Referring now to FIG. 5, a block diagram of a typical computer system which may employ the present invention is illustrated. The computer system 200 is controlled by a central processing system 202. The central processing system 202 includes a central processing unit such as a microprocessor or microcontroller for executing programs, performing data manipulations and controlling the tasks of the computer system 200. Communication with the central processing system 202 is implemented through a system bus 210 for transferring information among the components of the computer system 200. The bus 210 may include a data channel for facilitating information transfer between storage and other peripheral components of the hardware system. The bus 210 further provides the set of signals required for communication with the central processing system 202 including a data bus, address bus, and control bus. The bus 210 may comprise any state of the art bus architecture according to promulgated standards, for example industry standard architecture (ISA), extended industry standard architecture (EISA), Micro Channel Architecture (MCA), peripheral component interconnect (**PCI**) local bus, standards promulgated by the Institute of Electrical and Electronics Engineers (IEEE) including IEEE 488 general-purpose interface bus (GPIB), IEEE 696/S-100, and so on. Other components of the computer system 200 include main memory 204, auxiliary memory

206, and an auxiliary processing system 208 as required. The main memory 204 provides storage of instructions and data for programs executing on the central processing system 202. The main memory 204 is typically semiconductor based memory such as dynamic random access memory (DRAM) and or static random access memory (SRAM). The auxiliary memory 206 provides storage of instructions and data that are loaded into the main memory 204 before execution. The auxiliary memory 206 may include semiconductor based memory such as read-only memory (ROM), programmable read-only memory (PROM) erasable programmable read-only memory (EPROM), electrically erasable read-only memory (EEPROM), or flash memory (block oriented memory similar to EEPROM). The auxiliary memory 206 may also include a variety of non-semiconductor based memories, including but not limited to magnetic tape, drum, floppy disk, hard disk, optical, laser disk, **compact** disc read-only memory (CD-ROM), digital versatile disk read-only memory (DVD-ROM), digital versatile disk random-access memory (DVD-RAM), etc. Other varieties of memory devices are contemplated as well. The computer system 200 may optionally include an auxiliary processing system 208 which may be a digital signal processor (a special-purpose microprocessor having an architecture suitable for fast execution of signal processing algorithms), a back-end processor (a slave processor subordinate to the main processing system), an additional microprocessor or controller for dual or multiple processor systems, or a coprocessor.